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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,075	11/14/2003	John F. Zumkehr	42P17976	2622

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EXAMINER	
CHANG, DANIEL D	

ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/714,075	ZUMKEHR ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-20 and 22-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,6 and 24-35* is/are allowed.

6)☒ Claim(s) *2-4,7-20,22,23 and 36-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/28/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on September 28, 2005 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 2-4, 7-20, 22, 23, and 36-39 are rejected under 35 U.S.C. 102(e) as being anticipated by Zumkehr et al. (US 2004/0123207 A1, hereinafter "Zumkehr")

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Regarding Claim 2, Zumkehr discloses, in Figs. 3 and 4B, an integrated circuit to interface to memory (DDR memory 350 in Fig. 3), the integrated circuit comprising:

a first off chip driver calibration terminal (a terminal coupled to upper 406; such as 226 shown in Fig. 4A; see last sentence in paragraph 0043) to couple to an external pull-up resistor (415);

a second off chip driver calibration terminal (a terminal coupled to lower 406; such as 227 shown in Fig. 4A) to couple to an external pull-down resistor (416);

a first switch (upper 406) coupled between the first off chip driver calibration terminal and a voltage reference node (a node coupled between upper and lower 406 where VREF is connected to); and

a second switch (lower 406) coupled between the second off chip driver calibration terminal and the voltage reference node;

wherein the first switch and the second switch are selectively closed (paragraph 0043) to generate an internal voltage reference on the voltage reference node with which an input signal (DQ 120) is compared (420) in order to receive data.

Regarding Claim 3, Zumkehr discloses, in Fig. 4B, that the first switch is selectively closed and the second switch is selectively opened to generate a pull-up calibration voltage on the voltage reference node to calibrate an off-chip driver (paragraph 0043).

Regarding Claim 4, Zumkehr discloses, in Fig. 4B, that the first switch is selectively opened and the second switch selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the off-chip driver (paragraph 0043).

Regarding Claim 7, Zumkehr discloses, in Figs. 3 and 4B, an integrated circuit to interface to memory (DDR memory 350 in Fig. 3), the integrated circuit comprising:

a first off chip driver calibration terminal (a terminal coupled to upper 406; such as 226 shown in Fig. 4A; see last sentence in paragraph 0043) to couple to an external pull-up resistor (415);

a second off chip driver calibration terminal (a terminal coupled to lower 406; such as 227 shown in Fig. 4A) to couple to an external pull-down resistor (416);

a first switch (upper 406) coupled between the first off chip driver calibration terminal and a voltage reference node (a node coupled between upper and lower 406 where VREF is connected to); and

a second switch (lower 406) coupled between the second off chip driver calibration terminal and the voltage reference node;

a switch controller (340 in Fig. 3) having a mode input (inherent in order to activate the noise margin adjustment circuit 340), a first control output coupled to a control input of the first switch, and a second control output coupled to a control input of the second switch (inherent in order to control the switch 406), the switch controller control the opening and closing of the first switch and the second switch in response to the mode input (see paragraph 0043).

Regarding Claim 8, Zumkehr discloses, in Figs. 3 and 4B, that the first switch (upper 406) and the second switch (lower 406) are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal is compared in order to receive data (DQ 120); the first switch (upper 406) is selectively closed and the second switch (lower 406) is selectively opened to generate a pull-up calibration voltage on the voltage

reference node to calibrate an off-chip driver; and the first switch (upper 406) is selectively opened and the second switch (lower 406) is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the off-chip driver (see paragraph 0043).

Regarding Claim 9, Zumkehr discloses, in Fig. 4B, that the integrated circuit is a memory controller (300 in fig. 3).

Regarding Claim 10, Zumkehr discloses, in Figs. 3 and 4B, that the integrated circuit is a processor (see paragraph 0030-0032).

Method claims 11-15 are essentially the same in scope as apparatus claims 2-4 and 7-8 and are rejected similarly.

Regarding Claim 16, Zumkehr discloses, in Figs. 1A, 1B, 3, and 4B, a processor (102, 150, 152) for executing instructions and processing data (inherent for a processor);

a double data rate memory device (350 in Fig. 3) to store data from the processor and to read data to the processor (Paragraph 0040);

an external pull-up resistor (415; see last sentence in paragraph 0043) having a first end coupled to a first power supply terminal (VDDQ);

an external pull-down resistor (416; see last sentence in paragraph 0043) having a first end coupled second power supply terminal(Ground); and

a memory controller (300 in Fig. 3) coupled between the double data rate memory device and the processor, the memory controller including

a pull-up calibration terminal (a terminal coupled to upper 406; such as 226 shown in Fig. 4A) coupled to a second end of the external pull-up resistor,

a pull-down calibration terminal (a terminal coupled to lower 406; such as 227 shown in Fig. 4A) coupled to a second end of the external pull-down resistor,

a voltage reference node (a node coupled between upper and lower 406 where VREF is connected to),

a first switch (upper 406) having a first switch connection coupled to the pull-up calibration terminal and a second switch connection coupled to the voltage reference node, and

a second switch (lower 406) having a first switch connection coupled to the pull-down calibration terminal and a second switch connection coupled to the voltage reference node.

Regarding claim 17, Zumkehr implicitly discloses that the memory controller is an integrated circuit separate from the processor (see paragraph 0028 and 0030-0032).

Regarding claim 18, Zumkehr implicitly discloses that the processor is an integrated circuit and includes the memory controller (see paragraph 0028 and 0030-0032).

Regarding Claim 19, Zumkehr discloses, in Figs. 1A, 1B, 3, and 4B, that the memory controller further includes a switch controller (340 in Fig. 3) having a mode input (inherent in order to activate the noise margin adjustment circuit 340), a first control output coupled to a control input of the first switch, and a second control output coupled to a control input of the second switch (inherent in order to control the switch 406), the switch controller control the opening and closing of the first switch and the second switch in response to the mode input (see paragraph 0043).

Regarding Claim 20, Zumkehr discloses, in Figs. 1A, 1B, 3, and 4B, that the first switch and the second switch are selectively closed (see paragraph 0043) to generate an internal voltage

reference (voltage at a node between upper and lower 406) on the voltage reference node with which an input signal (DQ 120) is compared (420) in order receive data;

the first switch is selectively closed and the second switch is selectively opened (see paragraph 0043) to generate a pull-up calibration voltage on the voltage reference node to calibrate (paragraph 0045) a driver of the DDR memory device (see 350 in Fig. 3); and

the first switch is selectively opened and the second switch is selectively closed (see paragraph 0043) to generate a pull-down calibration voltage on the voltage reference node to further calibrate (paragraph 0045) the driver of the DDR memory device (see 350 in Fig. 3).

Regarding Claim 22, Zumkehr discloses, in Figs. 1A, 1B, 3, and 4B, a processor (102, 150, 152) for a computer system (see paragraph 0025, 0029), the processor including:

a memory controller (300 in Fig. 3) to interface to memory, the memory controller having

a pull-up calibration terminal (a terminal coupled to upper 406; such as 226 shown in Fig. 4A) to couple to an external pull-up resistor (415; see last sentence in paragraph 0043),

a pull-down calibration terminal (a terminal coupled to lower 406; such as 227 shown in Fig. 4A) to couple to an external pull-down resistor (416; see last sentence in paragraph 0043),

a voltage reference node (a node coupled between upper and lower 406 where VREF is connected to),

a first switch (upper 406) coupled between the pull-up calibration terminal and the voltage reference node,

a second switch (lower 406) coupled between the pull-down calibration terminal and the voltage reference node, and

a switch controller (340 in Fig. 3) having a mode input (inherent in order to activate the noise margin adjustment circuit 340), a first control output coupled to a control input of the first switch, and a second control output coupled to a control input of the second switch (inherent in order to control the switch 406), the switch controller control the opening and closing of the first switch and the second switch in response to the mode input (see paragraph 0043).

Regarding Claims 23 and 39, Zumkehr discloses, in Figs. 1A, 1B, 3, and 4B, that the first switch and the second switch are selectively closed (see paragraph 0043) to generate an internal voltage reference (voltage at a node between upper and lower 406) on the voltage reference node with which an input signal (DQ 120) is compared (420) in order receive data from a driver of a DDR memory device (see 350 in Fig. 3);

the first switch is selectively closed and the second switch is selectively opened (see paragraph 0043) to generate a pull-up calibration voltage on the voltage reference node to calibrate (paragraph 0045) the driver of the DDR memory device (see 350 in Fig. 3); and

the first switch is selectively opened and the second switch is selectively closed (see paragraph 0043) to generate a pull-down calibration voltage on the voltage reference node to further calibrate (paragraph 0045) the driver of the DDR memory device (see 350 in Fig. 3).

Regarding Claims 36-38, Zumkehr discloses, in Figs. 3 and 4B, that the first switch (upper 406) and the second switch (lower 406) are selectively closed to generate an internal voltage reference on the voltage reference node with which an input signal is compared in order to receive data (DQ 120); the first switch (upper 406) is selectively closed and the second switch (lower 406) is selectively opened to generate a pull-up calibration voltage on the voltage reference node to calibrate an off-chip driver; and the first switch (upper 406) is selectively

opened and the second switch (lower 406) is selectively closed to generate a pull-down calibration voltage on the voltage reference node to further calibrate the off-chip driver (see paragraph 0043).

Allowable Subject Matter

Claims 5, 6, and 24-35 are allowable over the prior art.

The following is a statement of reasons for the indication of allowable subject matter: the best prior art of record, Zumkehr, taken alone or in combination of other references, does not teach or fairly suggest an integrated circuit comprising, among other things, a plurality of input receivers each having a first input coupled to the voltage reference node and a second input coupled to a respective data terminal of a plurality of data terminals (claim 5); a first plurality of field effect transistors having sources coupled in parallel together to the first off-chip driver calibration terminal and drains coupled in parallel together to a voltage reference node; and a second plurality of field effect transistors having drains coupled in parallel together to the second off-chip driver calibration terminal and sources coupled in parallel together to the voltage reference node (claim 24); as set forth in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Timothy Callahan can be reached on (571)272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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